Chenhao Zhang

Phone: (585)748-6613 Email: chenhao7@andrew.cmu.edu Linkedin: https://www.linkedin.com/in/chenhao-zhang03/

EDUCATION

Carnegie Mellon University, Pittsburgh, PA

Master of Science in Computer Engineering 08/2025 – 12/2026

Purdue University, West Lafayette, IN

Bachelor of Science in Computer Engineering with highest distinction 09/2022 – 08/2025

- Honors: Purdue Engineering Dean's List and Semester Honors
- GPA: 4.00/4.00

COURSE PROJECT

Out-of-Order Processor – Issue Queue, Reorder buffer, and Register renaming (System Verilog) 09/2025 – Present

- Designed and implemented an issue queue that issues the in-order instructions in an out-of-order manner to the execution unit.
- Designed and implemented a reorder buffer that collects the finished instructions from the execution units, reorders them, and commits them in an in-order manner to ensure the correctness of execution.
- Designed and implemented register renaming to resolve the stall led by false dependencies, which are the Write-after-Read (WAR) and Write-after-Write (WAW) hazards.
- Currently working on the integration of the Dual-core Processor design with the Out-of-Order Processor design.

Dual-core Processor (System Verilog) 09/2024 – Present

- Designed a high-performance pipelined dual-core RISC-V processor, and implemented a fully pipelined datapath with forwarding logic and hazard detection to resolve data hazards efficiently; implemented a 2 bit branch predictor to avoid wrong prediction flush and achieve higher IPC.
- Developed comprehensive cache solutions and memory controller, including the design of instruction, and data cache, as well as a cache coherence memory controller to ensure write atomicity across multiple cores; implemented LR-SC atomic instruction for lock mechanism.
- Integrated all components into a shared-memory RISC-V multicore system; verified with RTL simulation, gate level synthesis, and FPGA prototyping on the Intel Altera DE-02 Development board with Intel Quartus software.

USB 1.1 transmitter (System Verilog) 04/2024

- Designed, implemented, and verified the transmitter that can process the input from AHB-lite and output the correct D+ and D- signal.
- Transmitter module supports sending 5 types of data type: ACK, NACK, STALL, DATA0 and DATA1.
- Design, implementation and verification of FIFO RAM structure. FIFO RAM capable of storing 64 bytes of data at a time with first in first out data management.
- Integrated the design with USB receiver and AHB-lite to achieve a fully functional USB1.1 design.

APB-Slave UART Receiver SoC Peripheral (System Verilog) 03/2024

- Designed a UART receiver that follows the packet sequence of start-bit, 5/7/8 data bits, parity bit, stop bit. The UART receiver will also check for framing error and overrun error.
- Designed a APB-Slave that is similar to the ARM's AMBA Bus system design with two stages: addressing stage and data stage. It is typically designed for slow speed peripheral devices.
- Integrated design of APB and UART to become an APB-connected UART SoC peripheral module.

RELEVANT COURSEWORK

Computer Design and Prototyping, Intro to Computer Security, Microprocessor Systems and Interfacing, ASIC Design Lab, Data Structures, Artificial Intelligence, Intro to Data Mining, Probabilistic Method, Signals and Systems, Discrete Mathematics, Intro to Digital System Design.

SKILLS

SOFTWARE SKILLS

C, System Verilog, RISC-V assembly, Python, Java, C#, MATLAB, AMD Vivado, Intel Quartus.

HARDWARE SKILLS

STM32FC091, AMD Xilinx Artix 7 FPGA, AMD ZYNQ FPGA, Intel ALTERA DE02 FPGA.